Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-24. (canceled)

25. (currently amended) ~~An electronic~~ A chip package comprising:

a first semiconductor chip; ~~circuitry component having a top surface;~~

a second semiconductor chip ~~circuitry component over~~ joined with a top surface of said first semiconductor chip; ~~top surface;~~

a first insulating layer covering a sidewall of said second semiconductor chip ~~circuitry component~~ and said top surface of said first semiconductor chip, wherein said first insulating layer comprises a top surface substantially parallel to said top surface of said first semiconductor chip; and

a metal layer over ~~on~~ said top surface of said first insulating layer. ~~first ins ulating layer.~~

Claims 26 and 27 (canceled)

28. (currently amended) The chip ~~electronic~~ package of claim 25 further comprising a bump between said first and second semiconductor chips. ~~circuitry components.~~

29. (currently amended) The chip ~~electronic~~ package of claim 28 further comprising a second insulating layer between said first and second semiconductor chips ~~circuitry components~~ and enclosing said bump.

Claim 30. (canceled)

31. (currently amended) The chip ~~electronic~~ package of claim 25 further comprising a via through said first insulating layer and connecting said first semiconductor chip ~~circuitry component~~ and said metal layer.

32. (currently amended) The chip ~~electronic~~ package of claim 25, wherein said top surface of said first insulating layer has ~~a top surface comprising~~ a first region and a second region, said first region being over said second semiconductor chip, ~~circuitry component,~~ said second region being over said first semiconductor chip but not over said second semiconductor chip, ~~circuitry component,~~ wherein said first and second regions are substantially coplanar.

33. (currently amended) The chip ~~electronic~~ package of claim 32, wherein said metal layer is on said first and second regions.

34. (currently amended) The chip ~~electronic~~ package of claim 25 further comprising a first bump over said metal layer.

35. (currently amended) The chip ~~electronic~~ package of claim 25, wherein said second semiconductor chip ~~circuitry component~~ comprises a top surface and a bottom surface facing said top surface of said first semiconductor chip, ~~circuitry component,~~ said first insulating layer being further over said top surface of said second semiconductor chip. ~~circuitry component.~~

Claims 36-44. (canceled)

45. (currently amended) The chip ~~electronic~~ package of claim 34 further comprising a substrate and a second bump connected to a bottom surface of said substrate, wherein said first bump is connected to a top surface of said substrate.

46. (new) The chip package of claim 45 further comprising an underfill between said substrate and said first insulating layer and enclosing said first bump.

47. (new) The chip package of claim 25, wherein said metal layer is on said top surface of said first insulating layer.

48. (new) The chip package of claim 47 further comprising a bump on said metal layer.